Monolithically integrated silicon spin qubits and cryogenic CMOS circuits for quantum computing

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For realizing a large-scale quantum computer having tens of millions of physical qubits, silicon hole and electron spin qubits are one of the leading candidates. They benefit from decades of studies, having a very small circuit footprint per qubit, isotopically purified Si-28 providing nuclear-spin-free qubit environment, and extensive fabrication infrastructure. Even more importantly, the CMOS technology enables integration conventional logic circuits for qubit control and read-out on the same chip.

We recently measured highly tunable electron and hole double (DQD) quantum dots [1] embedded in a 64-channel low power cryoCMOS multiplexer [2]. This approach allowed us to measure several dozens of single hole and electron quantum dots and tunable hole and electron DQDs in the same cooldown. At 5.6K temperature, we found unprecedentedly low low-frequency charge noise, of the order of $22\mu eV/\sqrt{Hz}$ at 1 Hz in the few-electron DQD, and 28 $\mu eV/\sqrt{Hz}$ at 1 Hz in the few-hole DQD, that we correlated with the gate-stack and qubit environment improvements as compared to the state-of-the-art FinFET or nanowire transistor-like qubit geometries. Our findings paved the way for hot silicon spin qubits operating at the threshold of quantum error correction.